Ceramic transient voltage suppressors, CTVS

General technical information

Date: July 2014

1 Introduction and definition

1.1 Introduction

Despite its many benefits, one of the few drawbacks of semiconductor technology is the vulnerability of solid-state devices to overvoltages. Even voltage pulses of very low energy can produce interference and damage, sometimes with far-reaching consequences. So, as electronics makes its way into more and more applications, optimum overvoltage or transient suppression becomes a design factor of decisive importance.

EPCOS ceramic transient voltage suppressors (CTVS) have proven to be excellent protective devices because of their application flexibility and high reliability. CTVS with their extremely attractive price/performance ratio, are ideal components for limiting surge voltage and current as well as for absorbing energy.

This data book covers following CTVS: multilayer varistors (MLVs), ESD/EMI filters, CeraDiodes and leaded transient voltage/RFI suppressors (SHCVs) with integrated multilayer ceramic capacitors (MLCCs). Special types for automotive electrical systems, surge protection (e.g. telecom), low clamping and high-speed applications round off the product range.

Additionally EPCOS offers radial-leaded disks, block varistors, strap-leaded varistors and arrester blocks for power distribution applications. For further information visit www.epcos.com.

1.2 Definition

Ceramic transient voltage suppressors (CTVS) are voltage-dependent resistors with a symmetrical V/I characteristic curve (figure 2) whose resistance decreases with increasing voltage.
Because of their application as overvoltage protection devices, they are also often referred to as TVS (transient voltage suppressors) on silicon basis.

The equivalent electrical circuit diagram symbols for varistors and CeraDiodes are displayed in figure 1.
Connected in parallel with the electronic device or circuit that is to be guarded, CTVS form a low-resistance shunt when voltage increases above a CTVS type-specific threshold value and thus prevent any further rise in the transient overvoltage.

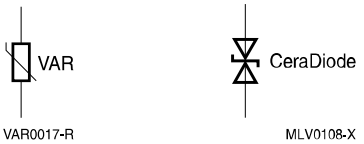

Figure 1
Circuit diagram symbols for a varistor and for a CeraDiode

1.3 Protection level

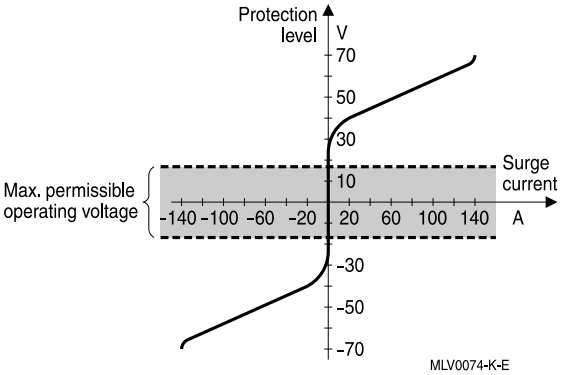

Figure 2
Protection level of the CTVS

The voltage dependence and protection level of CTVS or VDRs (voltage dependent resistors) in the switching mode may be approximately characterized by the formula

$$I = K \cdot V^{\alpha} \qquad \text{(equ. 1)}$$

where α denotes the “nonlinearity” exponent and in this way may be interpreted as a measure for the “steepness” of the V/I characteristic.
For CTVS it has been possible to produce α figures of more than 30. This places their protection levels in the same region as those of zener diodes and suppressor diodes. Exceptional current handling capabilities combined with fast response times make them an almost perfect protective device for transient overvoltages.

2 Construction

2.1 Multilayer CTVS (MLVs, ESD/EMI filters, CeraDiodes)

2.1.1 Multilayer ceramic body

The body of a multilayer CTVS consists of a stack of intercalating ceramic/electrode layers as shown in figure 3. The thickness of the ceramic layers affects the protection level.

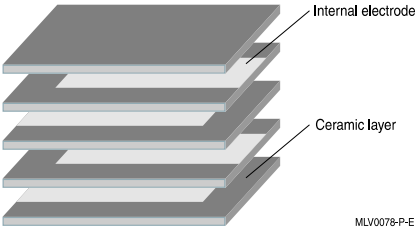

Figure 3
Construction of ceramic multilayers with printed electrodes

In the active volume of the ceramic body there are a number of internal electrode layers with an overlapping area affecting the pulse adsorption capability (figure 4). The internal electrodes are connected to the terminals or external electrodes. This is shown in figure 5 for chip and in figure 6 for array component.

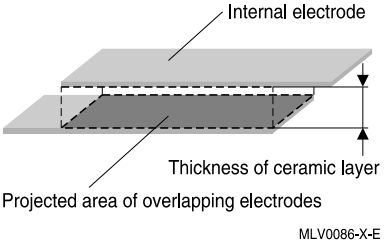

Figure 4
Design of ceramic layer

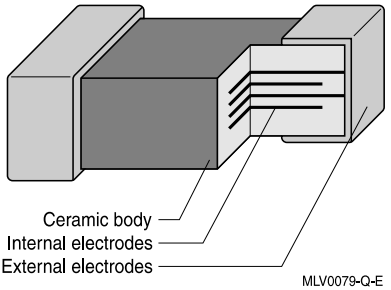

Figure 5
Internal construction of multilayer chip component

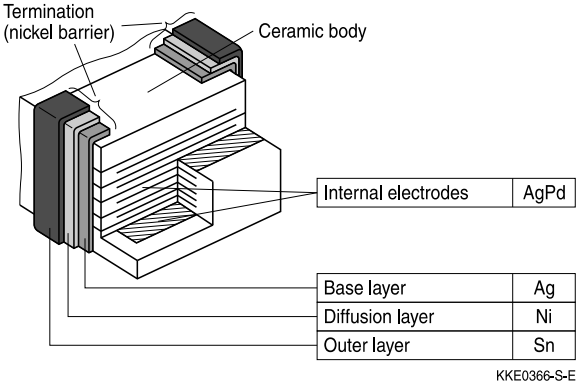

Figure 6
Internal construction of multilayer array component

2.1.2 Termination of multilayer components

2.1.2.1 Nickel barrier termination

The nickel barrier layer prevents leaching of the silver base metallization layer. The tin layer is needed to prevent oxidizing of the nickel layer and thus ensures better wetting by the solder. The nickel barrier termination is suitable for all commonly used soldering methods (see figure 7).

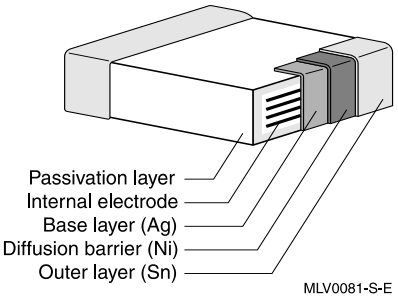

Figure 7
Ag/Ni/Sn termination of SMD multilayer chip component

2.1.2.2 Silver-platinum termination

The AgPt alloy termination is intended for lead-free reflow soldering (see figure 8).

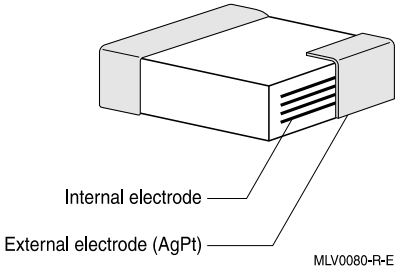

Figure 8
AgPt termination of SMD multilayer varistor

Note:
The robust construction of multilayer CTVS enables them to endure thermal stress without mechanical or electrical damage during common soldering processes.

2.1.3 Marking of multilayer components

There is no marking on multilayer components.

2.2 Leaded CTVS - leaded transient voltage/RFI suppressor (SHCV) series

2.2.1 Leaded CTVS body

This leaded product results from the combination of a multilayer capacitor and a multilayer varistor in one component. The final product is coated with a flame-retardant (to UL 94-V0) epoxy resin.

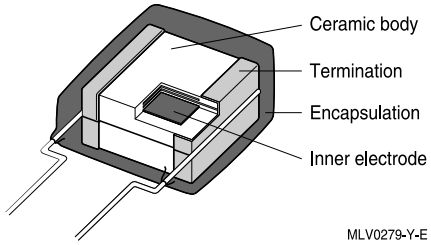

Figure 9
Construction of leaded CTVS component

2.2.2 Termination of SHCV

Tinned iron wires (RoHS-compatible), see figure 9.

2.2.3 Marking of SHCV

For further information refer to the corresponding data sheet.

2.2.4 Mechanical strength of wire leads of SHCV series

The wire leads comply with the requirements of IEC 60068-2-21. They may only be bent at a minimum distance of 4 mm from the enamel coating end. When bending leads to shape, the lead-component junction must be supported. The minimum bending radius should be 0.75 mm.

2.3 CTVS microstructure and conduction mechanism

Sintering zinc oxide (ZnO) together with other metal oxide additives under specific conditions produces a polycrystalline ceramic whose grain boundary resistance exhibits a non-linear dependence on voltage (figure 12). This phenomenon is called the varistor effect.

The electrical behavior of the multilayer CTVS, as indicated by figure 10, results from the number of microvaristors connected in series or in parallel.

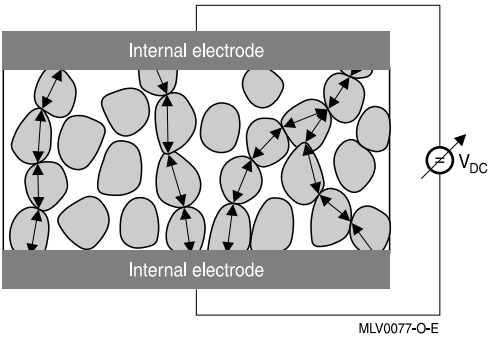

Figure 10
Conduction paths in the microstructure of multilayer CTVS

Figure 11 shows the microstructure of a CTVS ceramic consisting of ZnO grains and secondary phases like Bi_2O_3. The zinc oxide grains themselves are highly conductive, while the intergranular boundary formed of other oxides is highly resistive.

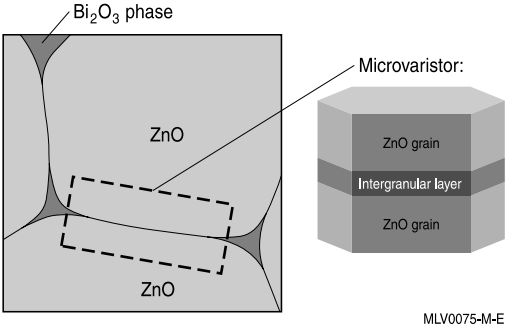

Figure 11
Microstructure of CTVS

At those points where zinc oxide grains are connected by an intergranular layer, sintering produces a microscopic structure or "microvaristor". The electrical characteristic of such a microvaristor is comparable to back to back connected semiconductor diodes (figure 12).

The series and parallel connection of the individual microvaristors in the sintered body of a CTVS also explains its high electrical load capacity compared to semiconductors. While the power in semiconductors is dissipated almost entirely in the thin p-n junction area, in a CTVS it is distributed over all the microvaristors, i.e. uniformly throughout the component's active volume. Each microvaristor is provided with energy absorbers in the form of zinc oxide grains with optimum thermal contact. This permits high absorption of energy and thus exceptionally high surge current handling capability.

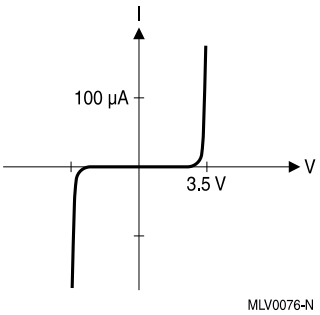

Figure 12
V/I characteristic of microvaristor

2.4 Electrical behavior and equivalent circuits

Figure 13 shows the simplified equivalent circuit of a multilayer varistor, valid for all CTVS. Use this circuit to interpret the behavior of a varistor for different current ranges.

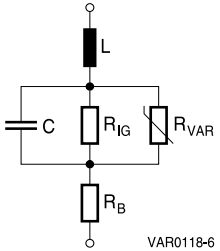

Figure 13
Equivalent circuit of a multilayer varistor

Legend:

L	Inductance
C	Capacitance
R_{IG}	Resistance of intergranular boundary ($\rho \approx 10^{12}$ to 10^{13} Ωcm)
R_{VAR}	Ideal varistor (0 to ∞ Ωcm)
R_B	Bulk resistance of ZnO ($\rho \approx 1$ to 10 Ωcm)

2.4.1 Low leakage current region

In the leakage current region the resistance of an ideal varistor goes towards ∞, so it can be ignored as the resistance of the intergranular boundary will predominate. Therefore $R_B \ll R_{IG}$, producing the equivalent circuit as in figure 14.

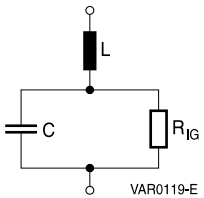

Figure 14
Equivalent circuit - low leakage current region

The ohmic resistance R_{IG} determines behavior at small currents, the V/I curve goes from exponential to linear (downturn region). R_{IG} shows a distinct temperature dependence, so a marked increase in leakage current must be expected as temperature increases.

2.4.2 Switching mode region

With $R_{VAR} \ll R_{IG}$ and $R_B \ll R_{VAR}$, R_{VAR} determines the electrical behavior (figure 15). The V/I curve (figure 17) follows to a good approximation the simple mathematical description by an exponential function (equation 3 in 2.5.1) where $\alpha > 30$, i.e. the curve appears more or less as a straight line on a log-log scale.

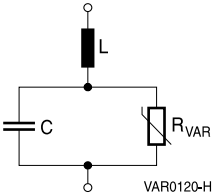

Figure 15
Equivalent circuit - breakdown region

2.4.3 High-current region (clamping region)

Here the resistance of the ideal varistor approaches zero. This means that

$R_{VAR} \ll R_{IG}$ and $R_{VAR} < R_B$ (figure 16).

The ohmic bulk resistance of ZnO causes the V/I curve to resume a linear characteristic (upturn region).

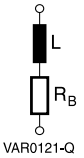

Figure 16
Equivalent circuit - breakdown region

Figure 17 illustrates the behavior of a CTVS and the different current regions.

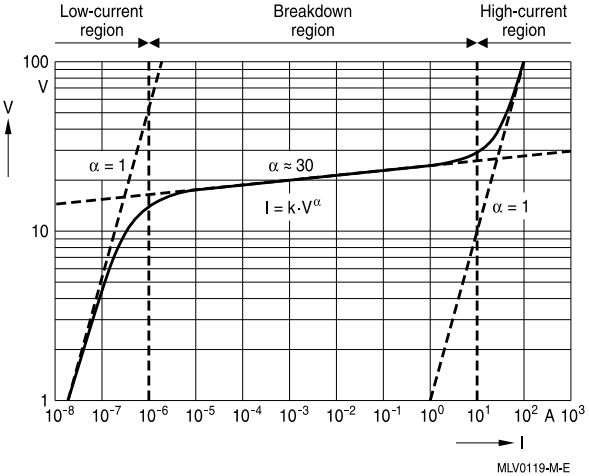

Figure 17
Operational modes

The CTVS V/I characteristics is explained in detail in the next section.

2.4.4 Capacitance

The equivalent circuit in figure 13 indicates the capacitance of CTVS components, refer to section 2.4.

2.4.5 Inductance

The equivalent circuit indicates the inductance of CTVS components.
The response time of the actual CTVS ceramics is in the picosecond region. Multilayer varistors, ESD/EMI filters and CeraDiodes have a very short response time (<0.5 ns) due to their low-inductance terminal design. For further details see also chapter "Protection standards," section 1.2.1 "Electrostatic discharge (ESD) to IEC 61000-4-2."
In the case of SHCVs, the inductance of the connecting leads causes the response time to increase to values of several nanoseconds. For this reason, all attempts must be made to achieve a mounting method with the lowest possible inductance, i.e. shortest possible leads.

2.5 CTVS V/I characteristics

2.5.1 Forms of presentation

The V/I characteristics of CTVS components are similar to those of power functions (odd exponents), so it is fairly obvious that the latter should be used to describe them (equation 1). As the curves are symmetrical, only one quadrant is generally shown for reasons of simplification (figure 18).

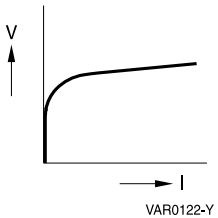

Figure 18
Presentation of V/I characteristics on a linear scale

$$I = K \cdot V^{\alpha} \qquad \alpha > 1 \qquad \text{(equ. 1)}$$

I Current through CTVS
V Voltage across CTVS
K Ceramic constant (depending on CTVS type)
α Nonlinearity exponent (measure of nonlinearity of curve)

Another possible interpretation of the physical principle underlying these curves is that of a voltage-dependent resistance value, and particularly its rapid change at a predetermined voltage (equation 2). This phenomenon is the basis of the CTVS protection principle (figure 19).

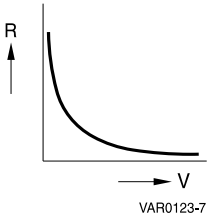

Figure 19
Presentation of R/V characteristics on a linear scale

$$R = \frac{V}{I} = \frac{V}{K \cdot V^{\alpha}} = \frac{1}{K} \cdot V^{1-\alpha} \qquad \text{(equ. 2)}$$

Equations 1 and 2 can be shown particularly clearly on a log-log scale, because power functions then appear as straight lines (see figure 20 and equation 3 or figure 21 and equation 4, respectively).

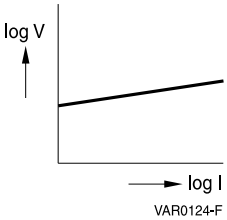

Figure 20
Presentation of V/I characteristics on a log-log scale

$$\log(I) = \log(K) + \alpha \cdot \log(V) \qquad \text{(equ. 3)}$$

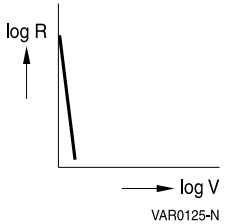

Figure 21
Presentation of R/V characteristics on a log-log scale

$$\log(R) = \log\left(\frac{1}{K}\right) + (1-\alpha)\log(V) \qquad \text{(equ. 4)}$$

This is virtually the only form of presentation used for CTVS characteristics (figures 20 and 21). A further advantage of the log-log format is the possibility of showing the wide range of the V/I curve (more than ten powers of 10).

It is evident that the simplified equations 1 to 4 cannot cover the downturn and upturn regions since they only describe the switching mode of the CTVS. Here a mathematical description as shown in equation 5 is required.

$$\log(V) = b1 + b2 \cdot \log(I) + b3 \cdot e^{-\log(I)} + b4 \cdot e^{\log(I)} \qquad I > 0 \qquad \text{(equ. 5)}$$

2.5.2 Determining the nonlinearity exponent α

Two pairs of voltage/current values (V_1/I_1 and V_2/I_2) are read from the V/I characteristic of the CTVS and inserted into equation 3, solved for α.

$$\log(I) = \log(K) + \alpha \cdot \log(V) \qquad \text{(equ. 3)}$$

$$\alpha = \frac{\log(I_2) - \log(I_1)}{\log(V_2) - \log(V_1)} \qquad \text{(equ. 6)}$$

Normally α is determined according to equation 6 from the pairs of values for 1 A and 1 mA of the V/I characteristic.

2.5.3 Presentation of the tolerance band

The real V/I characteristic of individual CTVS is subject to a certain deviation as shown in figure 22. This is primarily due to minor fluctuations in manufacturing and assembly process parameters. For CTVS belonging to a certain type, their V/I curves are required to lie entirely within a well defined tolerance band. The tolerance band shown in figure 22 illustrates this in the case of a multilayer varistor with voltage class K14 (MLV standard series, type CT0805K14G). Here voltage class K14 means the multilayer varistor having a maximum AC operating voltage of $V_{RMS,max}$ = 14 V and a varistor tolerance K of ±10 %.

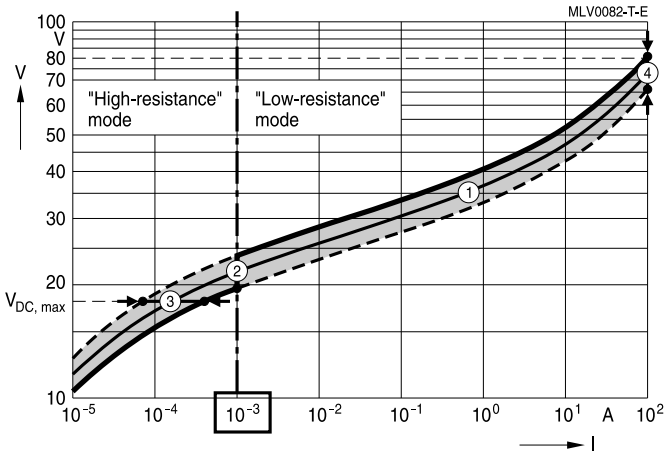

Figure 22
Tolerance limits in the V/I characteristic

CTVS are operated at one of two conditions. If the circuit is operated at normal operating voltage the CTVS has to be highly resistive. In an overvoltage event it has to be highly conductive.

These conditions concern two different segments of the CTVS V/I curve:

- Lefthand part of curve (<1 mA)
  This part of the curve refers to the “high-resistance” mode, where circuit designers may generally want to know about the largest possible leakage current at given operating voltage. Therefore the lower limit of the tolerance band is shown.
- Righthand part of the curve (>1 mA)
  This covers the “low-resistance” mode in an overvoltage event, where the circuit designer’s primary concern is about the worst-case voltage drop across the CTVS. The upper limit of the tolerance band is shown.

The 1 mA “dividing line” between those two segments does not really have electrophysical significance but is generally used as a standard reference for measuring the varistor voltage V_V also known as breakdown voltage V_{BR} (refer to data sheets CeraDiodes).

Example:

- Tolerance band
  Curve ① in the CTVS V/I characteristic (figure 22) shows the mean value of the tolerance band between the limits indicated by dashed lines. The mean at 1 mA represents the varistor voltage, in this case 22 V. The tolerance K ≙ ±10% refers to this value, so at this point the tolerance band ranges from 19.8 to 24.2 V (region ②).
- Maximum leakage current at operating voltage
  For the MLV standard series type CT0805K14G a maximum permissibe operating voltage of 18 V_{DC} is specified. Depending on the actual value of the MLV in the tolerance band (figure 22), you can derive a leakage current between $6 \cdot 10^{-6}$ A and $2 \cdot 10^{-4}$ A at room temperature (region ③). If the MLV is operated at a lower voltage, the figure for the maximum possible leakage current also drops (e.g. to max. $2 \cdot 10^{-6}$ A at 10 V_{DC}).
  In the worst case the peak value of the maximum permissible AC operating voltage ($v = \sqrt{2} \cdot 14 = 19.8$ V) will result in an ohmic peak leakage current of 1 mA.
- Maximum clamping voltage at surge current event (protection level)
  Assuming a surge current of 100 A, the voltage across this MLV will increase to between 65 V and 80 V (region ④), depending on the actual value of the MLV in the tolerance band.

2.6 Terms and descriptions

2.6.1 Operating voltage V_{op}

The product tables specify maximum AC and DC operating voltages. These figures should only be exceeded by transients. AUTO types (see MLV automotive E series), however, are rated to withstand excessive voltage (jump start) for up to 5 minutes.

The maximum permissible AC operating voltage is used to classify the individual voltage ratings within the type series.

In most applications the operating voltage is a given parameter, so the CTVS components in the product tables are arranged according to maximum permissible operating voltage to simplify comparison between the individual CTVS sizes.

2.6.2 Surge current, transient I_{surge}, surge voltage V_{surge}

Short-term current flow – especially when caused by overvoltage – is referred to as surge current or transient.

The maximum surge current $I_{surge,max}$ that can be handled by a CTVS depends on amplitude, pulse duration and number of pulses applied over device lifetime. The ability of a CTVS to withstand a single pulse of defined shape is characterized by the maximum non-repetitive surge current specified in the product tables.
If pulses of longer duration than 20 µs or multiple pulses are applied, the surge current must be derated as described in section 2.7.

2.6.2.1 Maximum surge current $I_{surge,max}$, maximum surge voltage $V_{surge,max}$

The maximum non-repetitive surge current is usually defined by an 8/20 µs waveform (rise time 8 µs/decay time to half value 20 µs) to IEC 62475 as shown in figure 23. This waveform approximates a rectangular wave of 20 µs. The derating curves of the surge current, defined for rectangular waveforms, consequently show a knee between horizontal branch and slope at 20 µs.
For telecom varistors (see surge protection series) the maximum surge current for a 10/700 µs surge voltage waveform (rise time 10 µs/decay time to half value 700 µs) to IEC 60060 is additionally defined. Further frequently used surge current and surge voltage waveforms are shown in the following table.

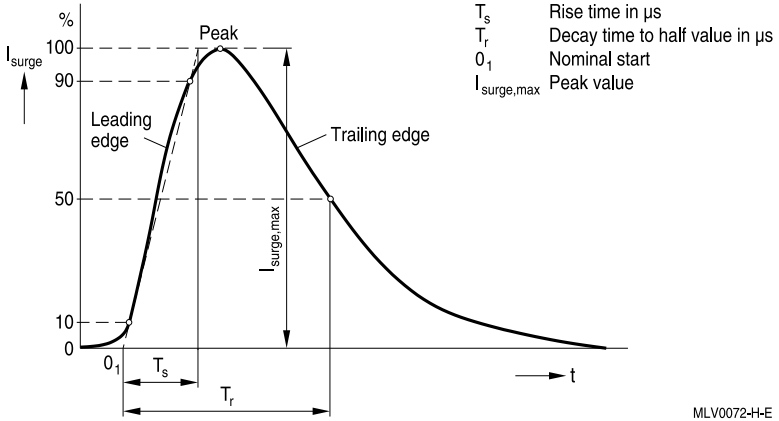

Figure 23
Waveforms to IEC 62475 standard

Frequently used T_s/T_r ratios

Surge currents	Surge voltages
4/10 µs	1.2/50 µs
8/20 µs	10/700 µs
10/350 µs	--
10/1000 µs	--

2.6.3 Energy absorption

The energy absorption of a CTVS is correlated with the surge current by

$$W = \int_{t_0}^{t_1} v(t) \cdot i(t)\, dt \qquad \text{(equ. 7)}$$

where v(t) is the voltage drop across the CTVS during current flow.

2.6.3.1 Maximum energy absorption W_{max}

Surge currents of relatively long duration are required to test maximum energy absorption capability. A rectangular wave of 2 ms to IEC 62475 (figure 24) is commonly used for this test.
In the product tables the maximum energy absorption is consequently defined for a surge current of 2 ms.

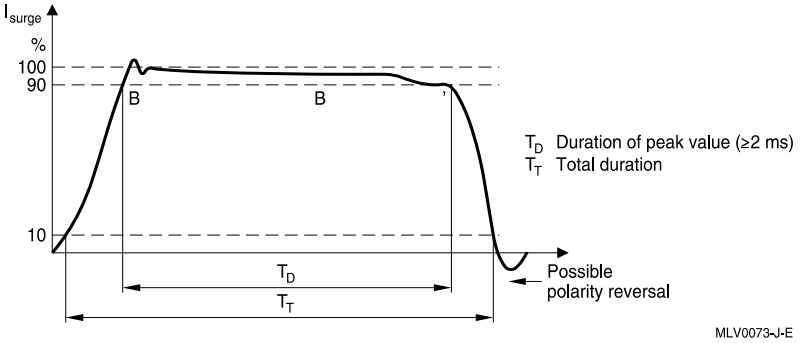

Figure 24
2 ms surge current waveform to IEC 62475 standard

2.6.4 Average power dissipation P_{diss}

If CTVS components are selected in terms of maximum permissible operating voltage, the resulting power dissipation will be negligible.

However, the rated maximum power dissipation must be taken into account if the varistor has not enough time to cool down between a number of surge pulses occurring within a specified isolated time period.

2.6.5 Varistor voltage V_V

The varistor voltage is the voltage drop across the CTVS when a current of 1 mA is applied to the device. It has no particular electrophysical significance but is often used as a practical standard reference in specifying overvoltage protection components. The tolerance of the varistor voltage refers to 25 °C.

Please note:
When the tolerance is examined, the current of 1 mA must only be applied briefly so that the results are not corrupted by warming of the CTVS (see section 2.6.10, "Temperature coefficient of V/I characteristic"). The current should only flow for 0.1 to 2.0 s, typical is a duration of 1 s.

2.6.6 Breakdown voltage V_{BR}

Breakdown voltage V_{BR} is used for CeraDiodes. If the diode voltage increases, e.g. due to ESD pulses, the voltage of the CeraDiode breaks down at a breakdown voltage V_{BR}. A current I_R then flows through the diode. The breakdown voltage V_{BR} is specified at a current of I_{BR} = 1 mA.

2.6.7 Protection level (clamping voltage) V_{clamp}

The protection level is the voltage drop across the CTVS for surge currents >1 mA. The V/I characteristics show the maximum protection level as a function of surge current (8/20 µs waveform). This is also referred to as clamping voltage V_{clamp}.

Comparing the protection behavior of CTVS components with semiconductors, higher figures of protection levels may be found for CTVS. For most state-of-the-art designs the protection level of CTVS components is more than sufficient.

2.6.7.1 Transmission line pulse (TLP) measurement

TLP measurement allows the accurate characterization of electronic protection devices such as MLVs or semiconductor diodes.
Here, electrical impulses are generated by means of a charged 50 Ω transmission line, then induced to the device via an attenuator and subsequent short 50 Ω transmission line; see figure 25.

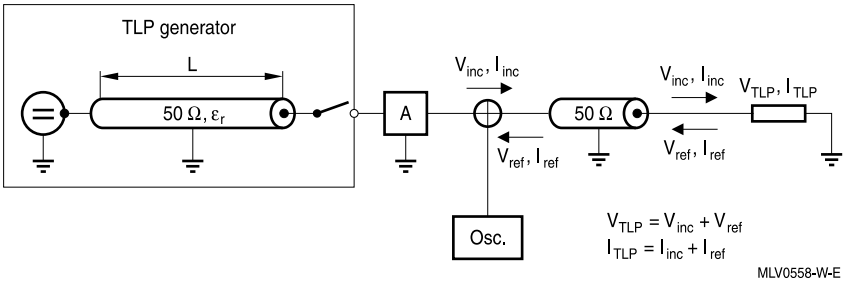

Figure 25
Test setup for TLP measurement

In contrast to test environments for ESD pulses according to standards such as IEC 61000-4-2 or 61000-4-5, impedance-matched transmission lines allow for distortion-minimized pulse propagation from the TLP generator to the device, due to the absence of parasitic capacitances or inductivities.
By these means it is possible to apply rather short pulses of clearly defined shape. Rectangular pulses of 100 ns width and rise times in the sub-ns region are commonly employed for TLP device characterization. Pulse width is dependent on generator transmission line length L and on wave propagation velocity v along the line.

$$T_{TLP} = \frac{2 \cdot L}{v} \qquad \text{(equ. 8)}$$

In turn, v amounts to the vacuum speed of light c_0, weighted by dielectric permittivity $\varepsilon_{r,TLP}$ of the transmission line cable, according to:

$$v = \frac{c_0}{\sqrt{\varepsilon_{r,TLP}}} \qquad \text{(equ. 9)}$$

T_{TLP}	[s]	Width of transmission line pulse
L	[m]	Length of generator transmission line
v	[m/s]	Wave propagation velocity of TLP
c_0	[m/s]	Vacuum speed of light
$\varepsilon_{r,TLP}$	[1]	Dielectric permittivity of transmission line cable

As the device under test usually represents a mismatch with the 50 Ω transmission line, incoming current I_{inc} and voltage V_{inc} will be partly reflected by the device, resulting in wave portions for both current I_{ref} and voltage V_{ref} that propagate in reverse direction toward the generator. Overall device voltage V_{TLP} and current I_{TLP} emerge from superposition of the respective incident and reflected waves. By proper dimensioning of the length of the transmission line end to the device, incident and reflected waves coincide at the attenuator exit during a limited time slot and are detected there by a dedicated oscilloscope.

The attenuator element suppresses any further impact of waves V_{ref} and I_{ref} that might be reflected again at the exit of the pulse generator and then head back to the measurement spot and, in other words, would dilute the results. Figure 26 shows the voltage response of a CTVS component on a TLP of 100 ns width.

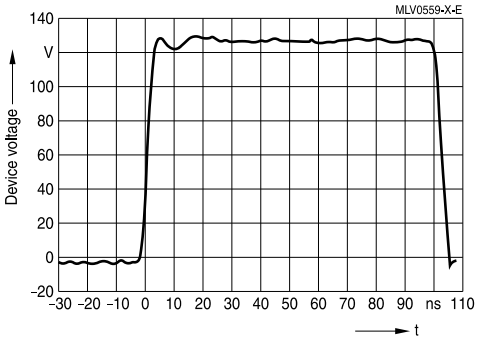

Figure 26
Voltage response of typical CTVS component on 100 ns transmission line pulse (TLP), shaped by means of NoiseKen INS-4040 generator and measured with LeCroy WaveRunner 104Xi high-speed oscilloscope.

The TLP method allows accurate recording of the V/I characteristics of protection devices especially in the high-current region, under clearly defined boundary conditions for the test pulse and environment (see figure 27). Short pulse widths avoid self-heating effects leading to damage of the tested devices. Furthermore, the onset time for the clamping behavior of the protection devices can be investigated accurately.

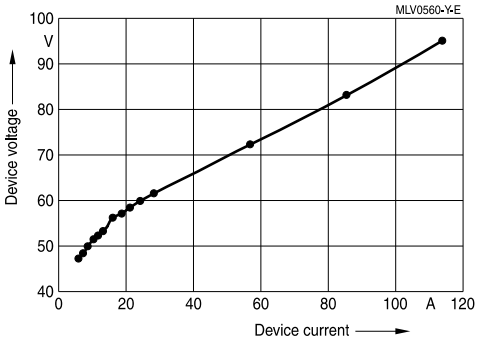

Figure 27
V/I characteristics of typical CTVS component in high-current region, obtained by TLP measurement.

The energy of the TLP pulse can be calculated according to equation 7, with v(t) denoting V_{TLP} and i(t) denoting I_{TLP}.

2.6.8 Capacitance

The product tables specify capacitance figures for measurement frequencies of 1 kHz or 1 MHz depending on the capacitance value. This is based on IEC 60384 standard for capacitors, where the measurement frequency decreases with increased capacitance value. The tabulated values show that CTVS components behave like multilayer ceramic capacitors with filtering properties similar to class 1 MLCCs.

In the data sheets we differentiate between specified (e.g. maximum) and typical capacitance values. Specified capacitance values represent a specific product characteristic. Typical capacitance values have an informational character, serve to provide a rough comparison of technically similar products and are not subject to outgoing inspection. The typical value range of parameters is not defined with specific upper and lower limits. Please contact your EPCOS representative if you have special requirements regarding specified values and tolerance ranges.

2.6.9 Response behavior, response time

The response time of CTVS ceramics to transients is in the subnanosecond region, i.e. varistors are fast enough to handle even ESD transients with the extreme steep current rise of up to 50 A/ns.

The CTVS components specified in this data book have the following response times:

SMD package (multilayer components)	<0.5 ns
Leaded package (SHCV series)	<25 ns

The reason for the different response time figures is the different series inductance of the package types (e.g. SMDs or leaded types), with lower inductance figures allowing for shorter response times.

This makes multilayer CTVS components ideal for ESD protection requirements. See also chapter "Protection standards," section 1.2.1, "Electrostatic discharge (ESD) to IEC 61000-4-2."

If surge currents with steep edges are to be handled, the circuit designer should always design the PCB layout for as low an inductance as possible.

2.6.10 Temperature coefficient of V/I characteristic

CTVS show a negative temperature coefficient of voltage. Figure 28 shows typical CTVS behavior.

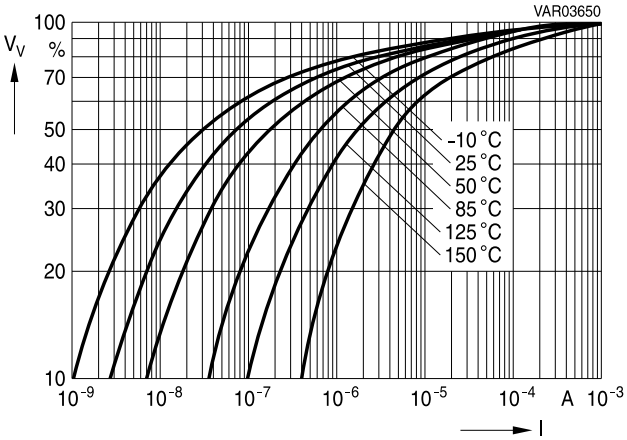

Figure 28
Typical temperature dependence of the V/I characteristic

The temperature coefficient drops with rising currents and is completely negligible from roughly 1 mA upwards. An increase in leakage current is consequently noticeable at higher temperatures, especially in the µA region.

Equation 10 describes the temperature coefficient of varistor voltage/breakdown voltage (at 1 mA):

$$|TC| < 0.5 \cdot 10^{-3}/K = 0.05\%/K = 1\%/\Delta 20\ K \qquad \text{(equ. 10)}$$

2.6.11 Temperature coefficient of capacitance

The typical temperature dependence of CTVS capacitance is shown in figure 29.

The typical temperature coefficient of CTVS capacitance is ≤0.1%/K.

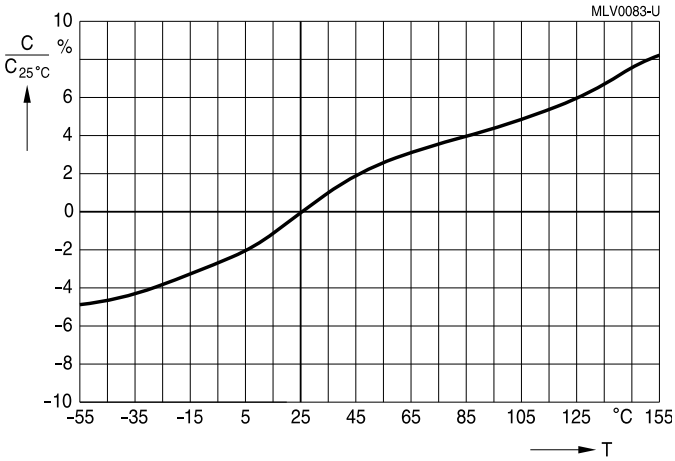

Figure 29
Temperature coefficient of CTVS capacitance

2.6.12 Operating temperature T_{op} and storage temperature T_{stg}

The limits of the operating and storage temperature ranges for the individual type series are specified in the product tables. If you consider operating the CTVS above the specified maximum operating temperature $T_{op,max}$, use the derating curves as explained in the next section.

2.7 Derating

Derating is the intentional reduction of maximum ratings in the application of a device. With CTVS components derating is of particular interest under the following conditions:

- derating for repetitive surge current and energy absorption
- derating at increased operating temperatures

2.7.1 Derating for repetitive surge current

A typical feature of CTVS components is the dependence of the maximum permissible ratings for surge current, and thus for energy absorption, on pulse shape, pulse duration, and the number of times this load is repeated during the overall lifetime of the CTVS.

The derating for a particular maximum permissible surge current can be derived from the curves for a type series in repetition figures graded 10^x. The surge derating curve is mainly dependent on the CTVS' case size but also on voltage rating. Such derating curves can be found in the data sheets.

The maximum permissible energy absorption can also be calculated from the derating curves by

$$W_{max} = V_{max} \cdot I_{surge,max} \cdot t_{r,max} \quad \text{(equ. 11)}$$

2.7.2 Derating at increased operating temperature

The following table comprises typical maximum specified operating temperatures for distinct CTVS series:

	$T_{op,max}$
CeraDiode series	+85 °C
Low clamping voltage series	+85 °C
ESD/ EMI filter series	+85 °C
Standard series	+125 °C
Automotive E series	+150 °C

To operate a CTVS at temperatures exceeding these figures (85 °C, 125 °C, or 150 °C) the following conditions have to be derated according to figure 30:

- maximum working voltage
- maximum surge current
- maximum energy absorption
- maximum average power dissipation

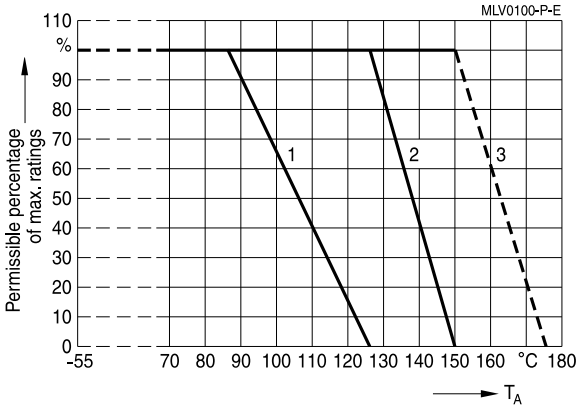

Figure 30
Derating curves

Derating curve 1	Derating curve 2	Derating curve 3
$T_{op,max}$ = 85 °C	$T_{op,max}$ = 125 °C	$T_{op,max}$ = 150 °C

For further details refer to product tables in the respective family data sheets.

2.7.3 Climatic categories

The limit temperatures according to IEC 60068 are stated in the product tables as LCT (lower category temperature) and UCT (upper category temperature).

2.8 Overload response

2.8.1 Moderate overload

Surge currents or continuous overload of up to approx. one and a half times the specified figures can lead to a change in varistor voltage/breakdown voltage by more than ±10%. In most cases the CTVS will not be destroyed, but there may be an irreversible change in its electrical properties and life time.

2.8.2 Heavy overload

Surge currents far beyond the specified ratings will puncture the CTVS element. In extreme cases the CTVS will burst.

Excessive steady-state overload fuses the ZnO grains and conducting paths are formed with the bulk resistance of ZnO, which is considerably lower than the resistance of the original CTVS. As a consequence the leakage current might be strongly increased over time ending in a short-circuit. The overload can overheat the CTVS ceramic to the effect that the surrounding PCB might burn or the CTVS becomes unsoldered from the electrodes (open circuit).

2.9 Storage

All EPCOS ceramic transient voltage suppressors must be used after shipment within the time specified:

Types	Storage time
CTVS types with nickel barrier termination	12 months
CTVS types with AgPt termination	6 months
Leaded CTVS types (SHCV series)	24 months

Here, the limiting factor is the solderability of the outer terminations. The properties of the varistor ceramic itself are not affected by storage.

Leave parts in the original packing to avoid any soldering problems caused by oxidized terminals.

For further details please refer to chapter "Soldering directions".

Storage temperature	−25 °C to 45 °C
Max. relative humidity (without condensation)	< 75% annual average < 95% on max. 30 days per annum

2.10 Prior damage

The values specified only apply to CTVS in delivery condition that have not been subjected to prior electrical, mechanical or thermal damage.