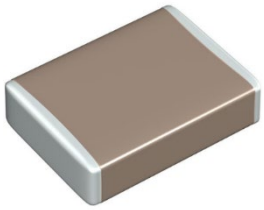
CeraLink

Ceramic capacitor for fast-switching power electronic circuits

Series/Type:	**2220**
Ordering code:	**B58043***
Date:	2024-03-27
Version:	3.0

Known customer applications

- Power converters and inverters
- DC link / snubber / filter capacitors for power converters and inverters



Features

- High ripple current capability
- High capacitance density
- Increasing capacitance with DC bias up to operating voltage
- No limitation dV/dt
- High temperature robustness with low losses at high temperature
- Low equivalent serial inductance (ESL) and resistance (ESR)
- Ideal for high frequencies up to several MHz
- Generally low self-heating and good thermal self-regulation properties
- Qualification based on AEC-Q200 Rev. E

Construction

- Multilayer technology
- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate, see RoHS exemption 7c-II). For detailed information please refer to the *TDK Environmental protection* website.
- Copper inner electrodes
- Nickel barrier termination (Cu/Ni/Sn), recommended for lead-free soldering and compatible with tin/lead solder
- Conductive resin layer between Cu and Ni layer (soft termination type only)

General technical data

Dissipation factor	$\tan\delta$	< 0.025	
Insulation resistance	$R_{ins,\ typ}$ *)	> 10	GΩ
Operating device temperature	T_{device}	-40 … +150	°C

*) Typical insulation resistance, measured at operating voltage V_{op} and measurement time ≥ 240 s, +25 °C

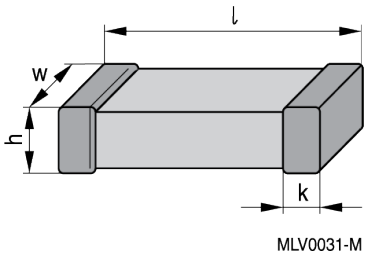
Electrical specifications and ordering codes

Termination	$V_{pk, max}$ V	V_R V	V_{op} V	$C_{nom, typ}$ nF	$C_{eff, typ}$ nF	C_0 nF	$C_{0, typ}^{unpoled}$ nF	Ordering code
Standard	650 (130% V_R)	500	400	250	150	85 ±20%	50	B58043I5254M052
Soft								B58043E5254M052
Standard	1080 (120% V_R)	900	800	56	33	20 ±20%	12	B58043I9563M052
Soft								B58043E9563M052

Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

Dimensional drawing



MLV0031-M

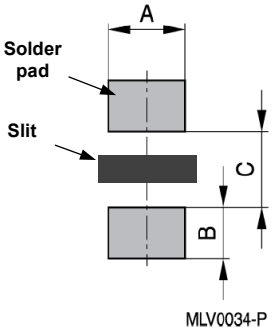
Case size EIA / mm	l	w	h	k	Ordering code
2220 / 5750	5.7 ±0.4	5.0 ±0.4	1.4 ±0.2	0.25 … 1.0	B58043*5254M052
			1.6 ±0.2		B58043*9563M052

Dimensions in mm

Recommended solder pad layout

Case size EIA / mm	A	B	C
2220 / 5750	5.5	1.5	4.2 *)

Dimensions in mm



MLV0034-P

*) Particularly for the 900 V type it is recommended to provide a slit (about 1 mm width) in the P.C. board under the component to increase creepage distance and improve washing of flux. Make sure to dry detergent up completely.

It is recommended to use low activated flux (Chlorine content: less than 0.1wt%) due to high voltage usage – see *Soldering directions* for details.

Depending on the expected contamination of the P.C. board in application a conformal coating might be necessary to meet normative requirements on creepage distance (in case of doubt regarding potential chemical intolerances please contact TDK).

Polarity and marking of components

In contrast to other CeraLink types, CeraLink 2220 components do not have a polarity marking.

Note that after reflow soldering, the components are usually unpoled due to temperature effects, where the re-poling happens automatically after switching on the operating voltage V_{op}.

If components are operated below the specified operating voltage V_{op}, a first-time poling is required to establish the specified capacitance values, see our *CeraLink Technical Guide* for further details.

Typical values as a design reference for CeraLink applications

Ordering code	Weight	ESR 0 V DC 0.5 V AC (RMS) 25 °C, 1 kHz	ESR 0 V DC 0.5 V AC (RMS) 25 °C, 1 MHz	ESL	I_{op} *) V_{op} 100 kHz T_{amb} = 85 °C	I_{op} *) V_{op} 100 kHz T_{amb} = 105 °C
	g	Ω	mΩ	nH	A (RMS)	A (RMS)
B58043I5254M052	0.26	15	40	3	5.0	4.3
B58043E5254M052					4.5	3.8
B58043I9563M052	0.29	54	160		2.4	2.1
B58043E9563M052					2.3	2.0

*) Normal operating current without forced cooling at T_{device} = +150 °C. Higher values permissible at reduced lifetime.

Application notes

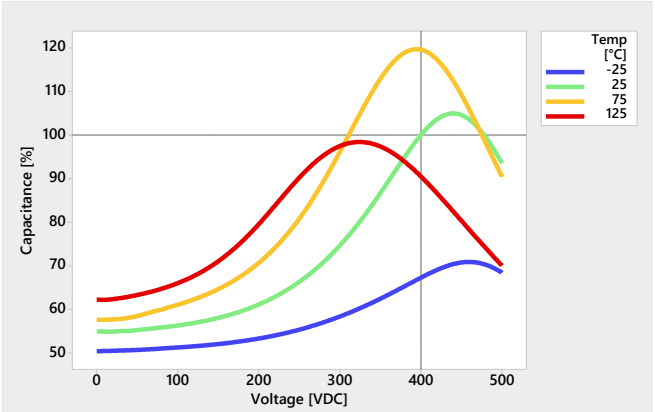
Further typical electrical characteristics as a design reference for CeraLink applications.

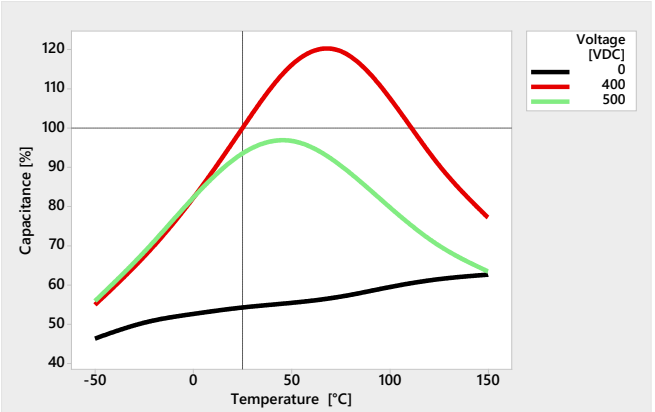
Typical characteristics as a function of temperature and voltage - V_R = 500 V

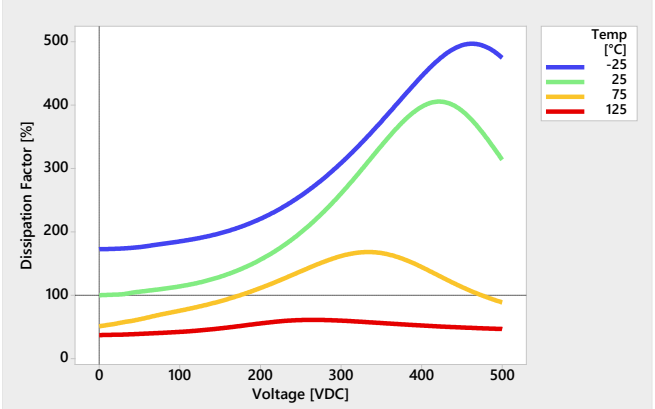
(0.5 V AC (RMS), frequency = 1 kHz)

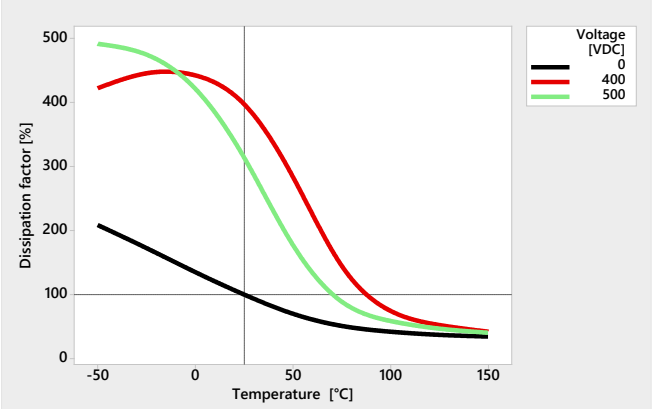
All given temperatures are device temperatures (measured on ceramic surface).

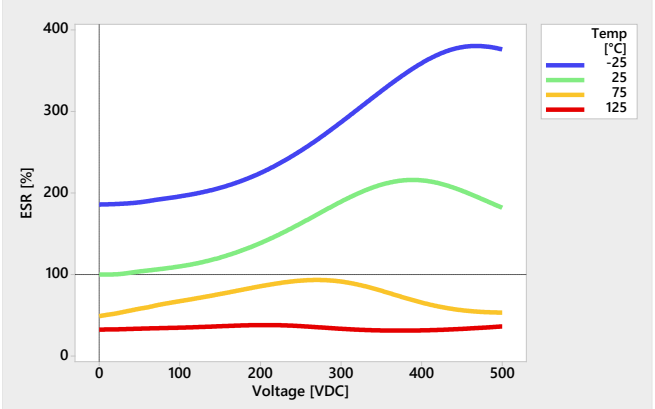
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tanδ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 4 of this data sheet.

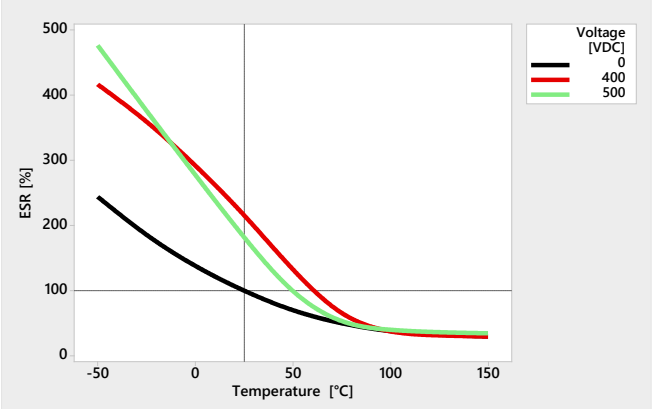










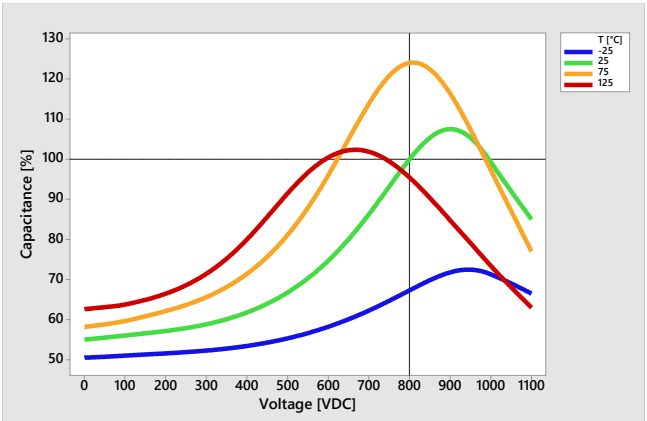


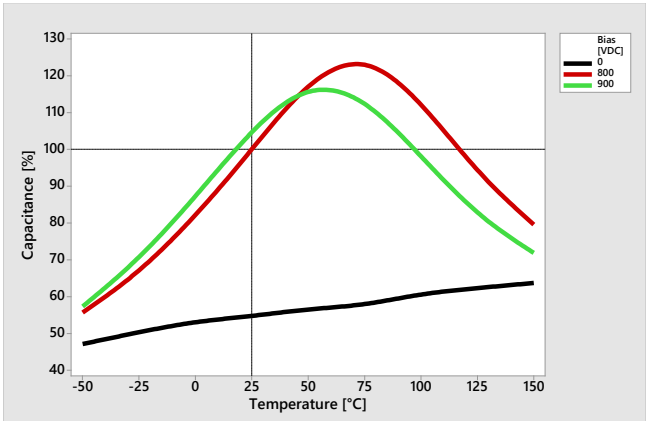
Typical characteristics as a function of temperature and voltage - V_R = 900 V

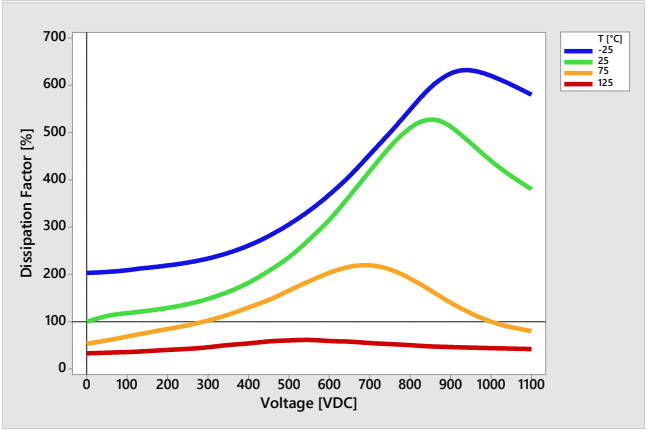
(0.5 V AC (RMS), frequency = 1 kHz)

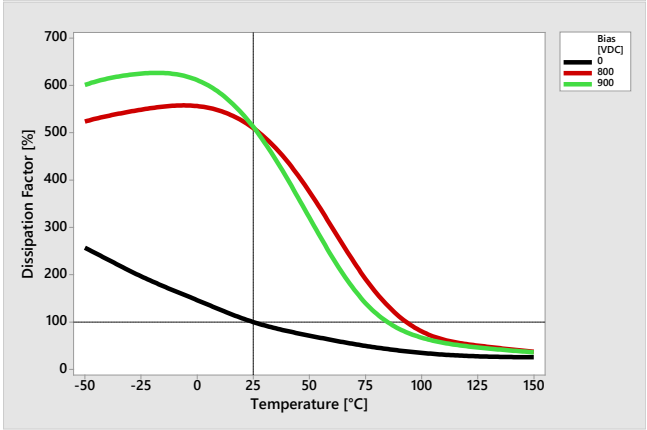
All given temperatures are device temperatures (measured on ceramic surface).

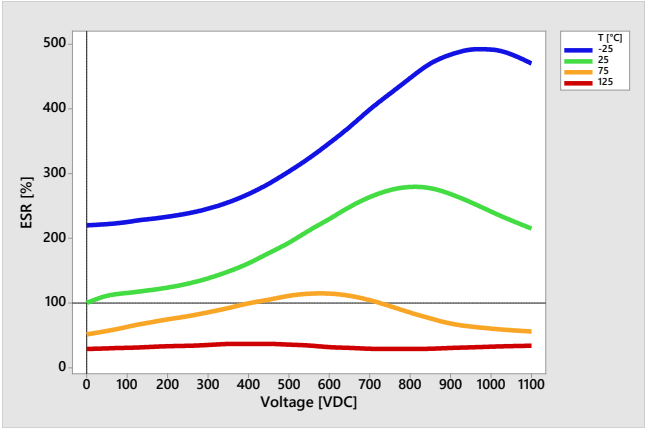
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to tan δ, $C_{eff, typ}$ and ESR_{1kHz} which are given on page 2, 3 and 4 of this data sheet.

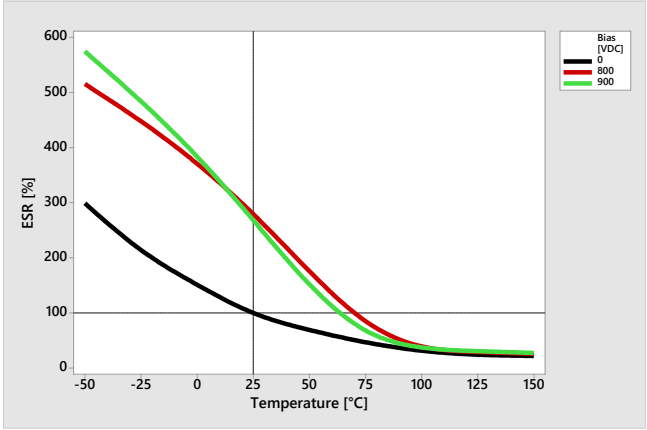












Further typical capacitance values as a function of voltage

Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C.

The nominal capacitance is defined as the large signal capacitance at V_{op}.

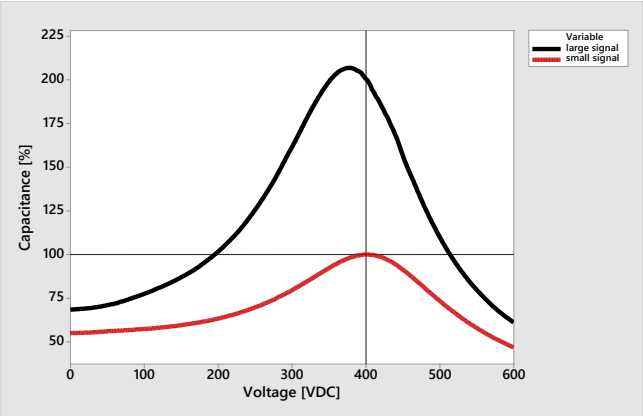
See glossary for further information.

Small signal capacitance:

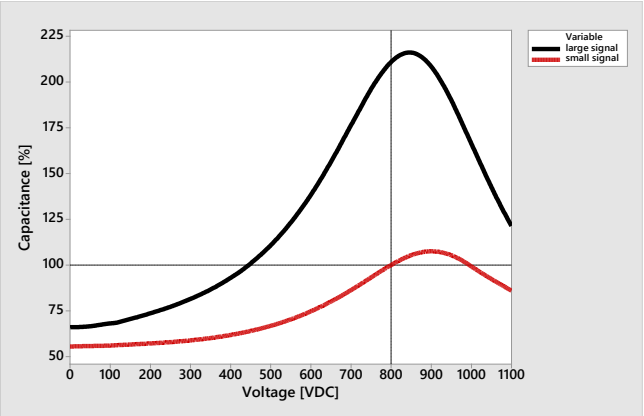
0.5 V AC (RMS), 1 kHz, +25 °C

The effective capacitance is defined as the small signal capacitance at V_{op}.

V_R = 500 V (B58043*5)**

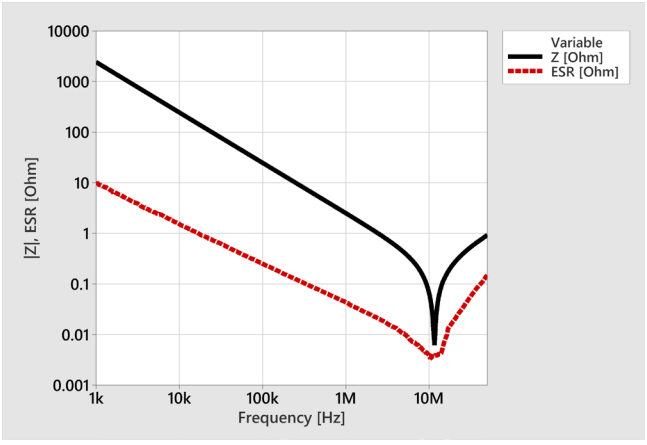


V_R = 900 V (B58043*9)**

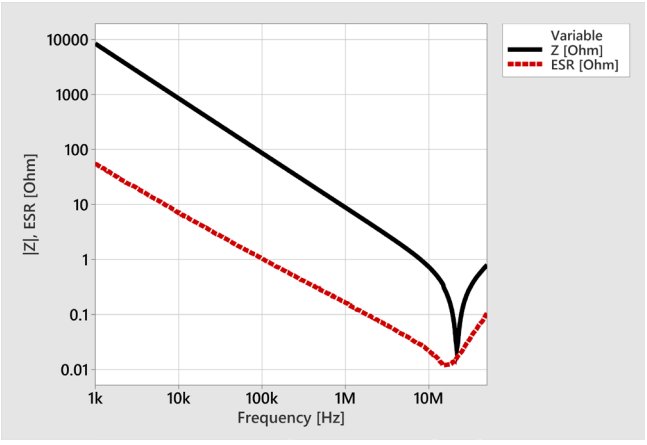


Typical impedance and ESR as a function of frequency

(0 V DC, 0.5 V AC (RMS), T_{device} = 25 °C)



B58043*5254M052



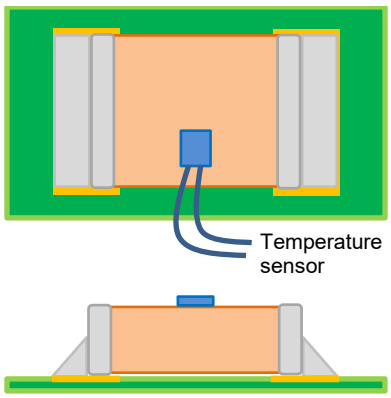
B58043*9563M052

Typical permissible current as a function of frequency

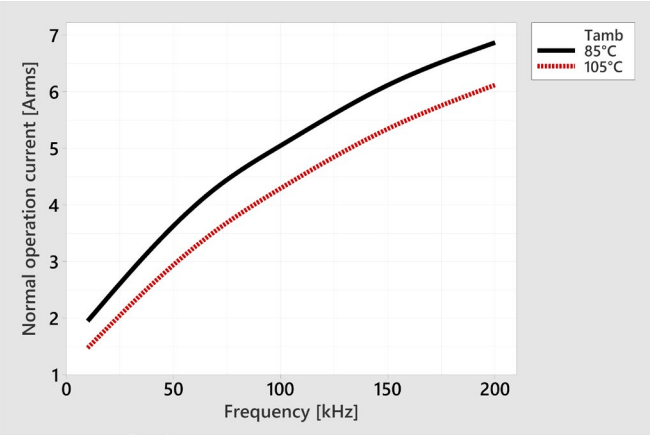
Measurement performed at V_{op} without forced cooling.

Note that with additional cooling the typical permissible current can be significantly higher.

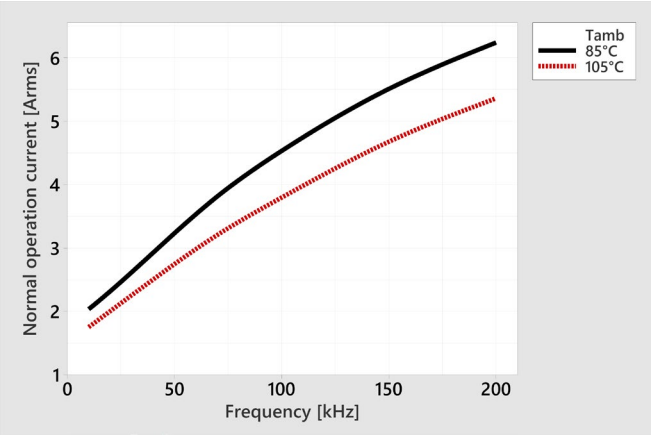
The given values correspond to a device temperature of 150 °C (measured on the ceramic surface).



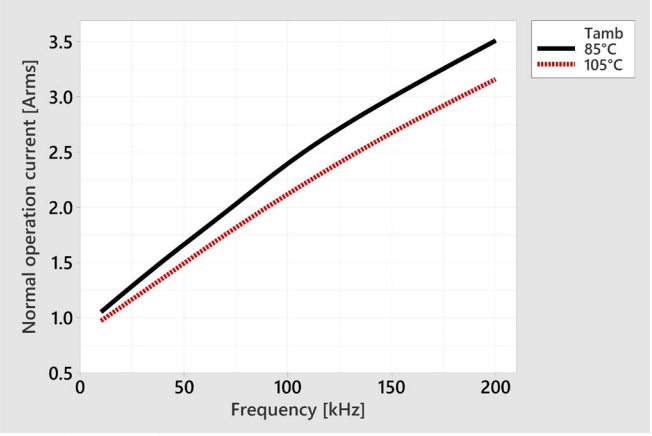
CL2220 500V Standard termination (B58043I5254M052)



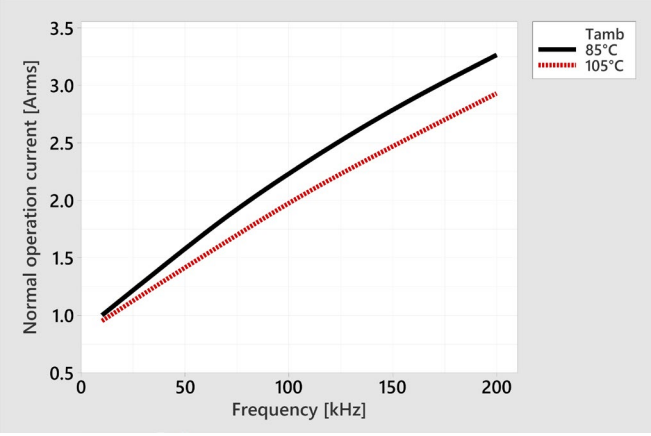
CL2220 500V Soft termination (B58043E5254M052)



CL2220 900V Standard termination (B58043I9563M052)

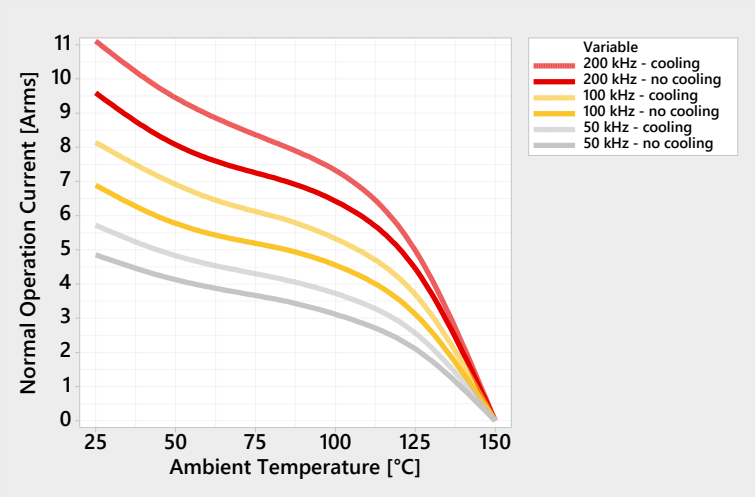


CL2220 900V Soft termination (B58043E9563M052)

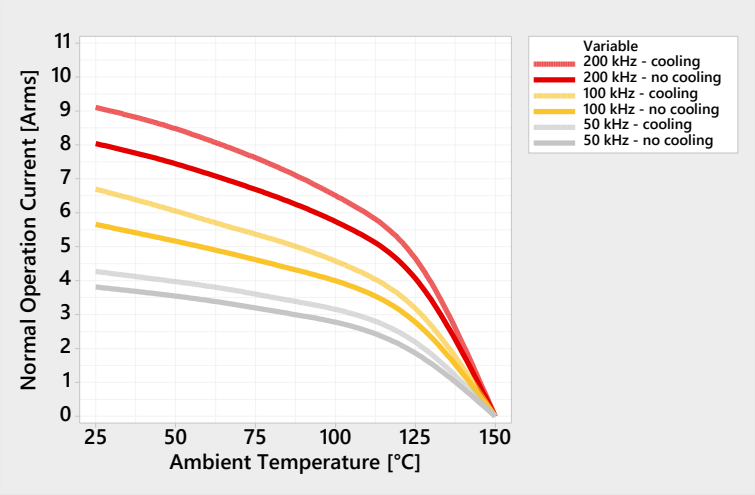


Typical permissible current as a function of ambient temperature

Standard termination type (B58043I5254M052)



Soft termination type (B58043E5254M052)



Measurement performed at V_{op}. The values correspond to a device temperature of 150 °C (measured on the ceramic surface).

Without forced cooling:

Component mounted on PCB without any heatsink nor active airflow (convection only)

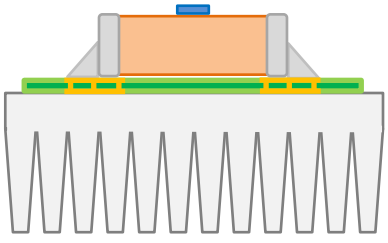
Without heatsink

With cooling:

Component mounted on PCB with additional heatsink (40 mm x 75 mm x 100 mm, aluminum, 1.2-1.4 K/W).

Heatsink is isolated from the PCB by a layer of Kapton® foil.

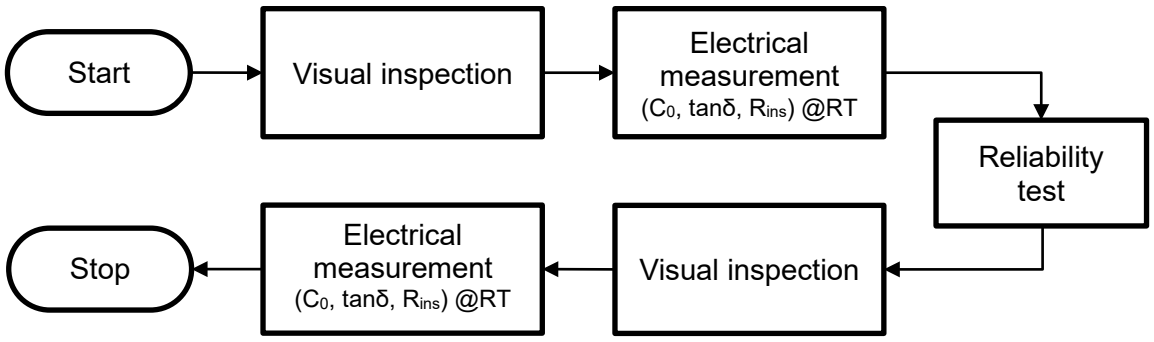
Moderate forced airflow is provided by the oven fan.



With heatsink

Reliability: Test methods and conditions

General test flow



Pre- and post-measurement for AEC-Q200 tests

A. Preconditioning:

- Reflow solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of isolation resistance R_{ins} *)

  Apply $V_{pk,max}$ for 7 seconds and measure R_{ins} at room temperature:
  Isolation resistance (@ $V_{pk,max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
- Measurement of electrical parameters C_0 and tanδ according to specification

  Measure C_0 and tanδ within 10 minutes to 1 hour afterwards:
  Initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **C_0 acc. spec. on page 3**
  Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tanδ < 0.025**

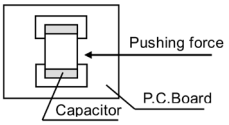
B. Performance of a specific reliability test.

C. After performing a specific test:

- Check the external appearance again
- Repeat the measurement of the electrical parameters
  - Apply $V_{pk,max}$ for 7 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@ $V_{pk,max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
  - Measure C and tanδ:
    Change of initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **$|\Delta C_0 / C_0| < 15\%$**
  - Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tanδ < 0.05**

*) Note that the measurement of the isolation resistance R_{ins} using the described measurement conditions is for pre- and post-measurement within the scope of the AEC-Q200 reliability tests only (see next page for details).

Test conditions and criteria

	Test	No	Test method	Test conditions	Criteria
Qualification tests based on AEC-Q200 Rev. E (Table 2)	Pre- and Post- Stress Electr. Test	1	-	As described above	Common failure criteria *).
	Temperature Cycling	4	JESD22-A-104	-55 °C to +150 °C, ≤ 20 secs transfer time, 15 mins dwell time, 1000 cycles	No mechanical damage. Common failure criteria *).
	Destructive Physical Analysis	5	EIA-469		No internal defects that might affect performance or reliability
	Biased Humidity	7	MIL-STD-202 Method 103	+85 °C, 85% rel. hum., V_R, 1000 hours	No mechanical damage. Common failure criteria *).
	High Temperature Operating Life (HTOL)	8	MIL-STD-202 Method 108	+150 °C, V_R, 1000 hours	No mechanical damage. Common failure criteria *).
	External Visual	9	MIL-STD-883 Method 2009	Visual inspection with magnifying glass	No external defects that might affect performance or reliability
	Physical Dimension	10	JESD22-B-100	Verify physical dimensions to the device specification using a caliper	Within specified tolerance
	Mechanical Shock	13	MIL-STD-202 Method 213	Acceleration: 100 g, half sine pulse, duration: 6 milliseconds, 3 shocks in each direction, 18 shocks in total	No mechanical damage. Common failure criteria *).
	Vibration	14	MIL-STD-202 Method 204	20 g / 20 min, 12 cycles, 3 axes, 10 Hz to 2000 Hz	No mechanical damage. Common failure criteria *).
	Resistance to Soldering Heat	15	See *Soldering directions*		
	ESD	17	AEC-Q200-002	HBM, ±25kV, 5 pulses each polarity	No mechanical damage. Common failure criteria *).
	Solderability	18	See *Soldering directions*		
	Electrical Characterization	19	-	See conditions for pre-measurement of AEC-Q200 tests on previous page	R_{ins}, C_0 and tanδ within defined limits.
	Board Flex	21	AEC-Q200-005	Bending of 2 mm for 60 seconds (5 mm for soft termination types)	No mechanical damage. Common failure criteria *).
	Terminal Strength (SMD)	22	AEC-Q200-006	Apply a force of 17.7 N for 60 seconds 	No detaching of termination. No rupture of ceramic. Common failure criteria *).
Other tests	Voltage proof	-		Withstand test voltage: V_R | Apply voltage 500 V | 150% V_R 900 V | 120% V_R Charge / discharge current: ≤ 50 mA	No insulation breakdown or other damage. R_{ins}, C_0 and tanδ within defined limits.

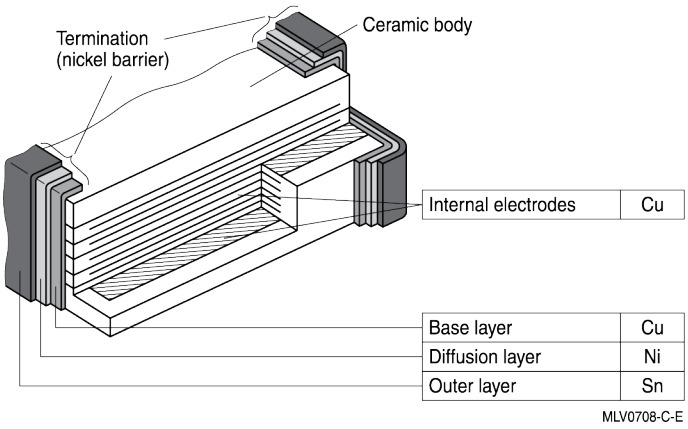
*) Common failure criteria: R_{ins}, $|\Delta C_0/C_0|$ and tanδ within defined limits (see pre- and post-measurement on prev. page).

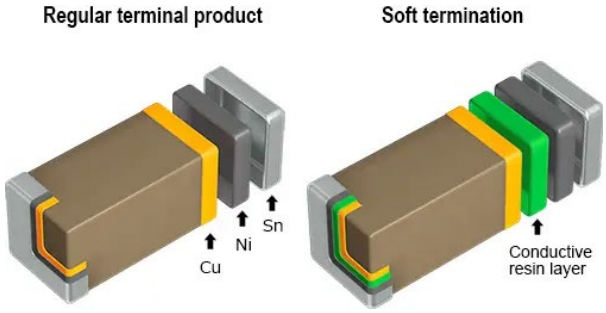
Internal design and termination

The CeraLink 2220 is a PLZT (lead lanthanum zirconium titanate) based ceramic capacitor with anti-ferroelectric behaviour, which is optimized for high frequency & high temperature power electronic applications (see our *CeraLink Technical Guide*) for further details. The internal chip design offers high capacitance density, where the copper inner electrodes provide excellent thermal dissipation such that high current capabilities can be achieved in applications.

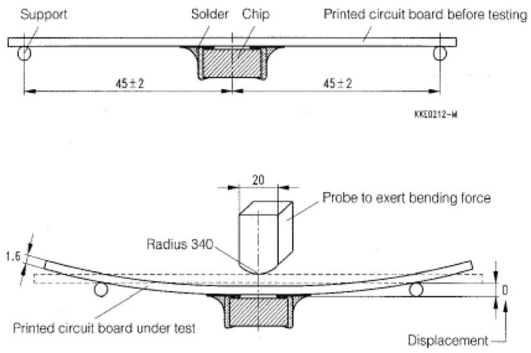
In addition to the standard copper/nickel/tin terminal electrode, CeraLink 2220 components are available also with soft termination. Soft termination is a type of flexible termination in which a conductive resin layer is provided between the Cu base and Ni plating layer. The resin layer absorbs stress accompanying expansion or shrinkage of the solder joints due to thermal shock or flex stress on the board and can prevent cracking of the capacitor element. Furthermore, it provides excellent performance in the AEC-Q200 board flex test as detailed below.

The nickel layer of the termination acts as a diffusion barrier and prevents leaching of the copper base metallization layer. This allows great flexibility in the selection of soldering parameters. The tin prevents oxidation of the nickel layer and thus facilitates better wettability of the soldering surface. The nickel barrier termination is designed for lead-free as well as Sn/Pb soldering (see *Soldering directions* for further details).

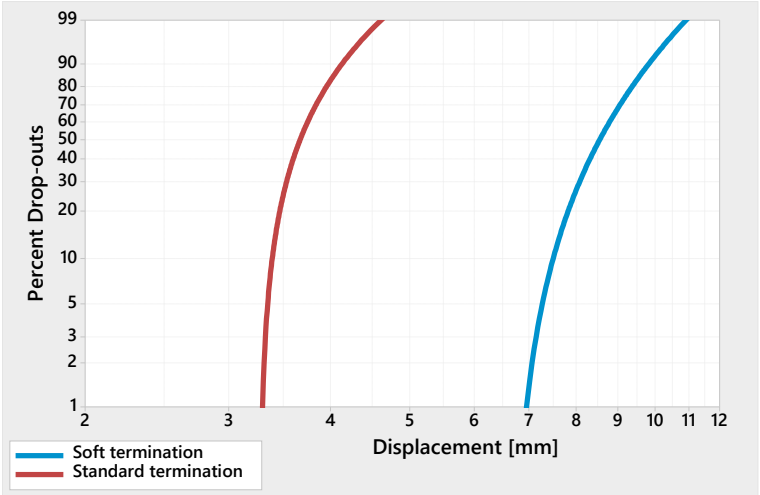




Typical bending test results for CeraLink 2220 for standard and soft termination



AEC-Q200 Rev. D - Method 005 - Board Flex Test

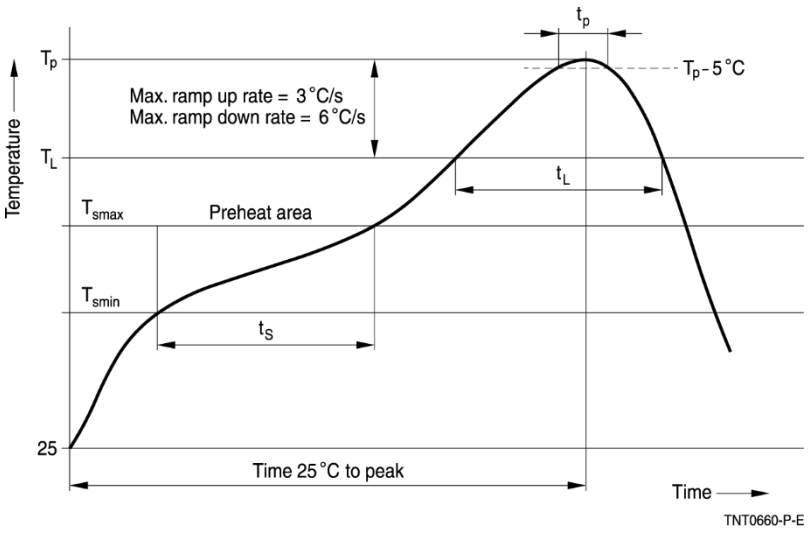


CeraLink 2220 (1.4 mm chip height)

Soldering directions

1. Recommended reflow soldering profiles

Temperature ranges for reflow soldering according to IEC 60068-2-58 recommendations.



Profile feature		Sn-Pb eutectic assembly	Pb-free assembly
Preheat and soak			
- Temperature min	T_{smin}	100 °C	150 °C
- Temperature max	T_{smax}	150 °C	200 °C
- Time	t_{smin} to t_{smax}	60 … 120 s	60 … 120 s
Average ramp-up rate	T_{smax} to T_p	3 °C/s max.	3 °C/s max.
Liquidous temperature	T_L	183 °C	217 °C
Time at liquidous	t_L	40 … 150 s	40 … 150 s
Peak package body temperature	T_p [1)]	215 °C … 260 °C [2)]	235 °C … 260 °C
Time (t_p) above (T_p -5 °C)	t_p [3)]	10 … 40 s	10 … 40 s
Average ramp-down rate	T_p to T_{smax}	6 °C/s max.	6 °C/s max.
Time 25 °C to peak temperature		max. 8 minutes	max. 8 minutes

[1)] Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
[2)] Depending on package thickness (cf. JEDEC J-STD-020D).
[3)] Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Notes:

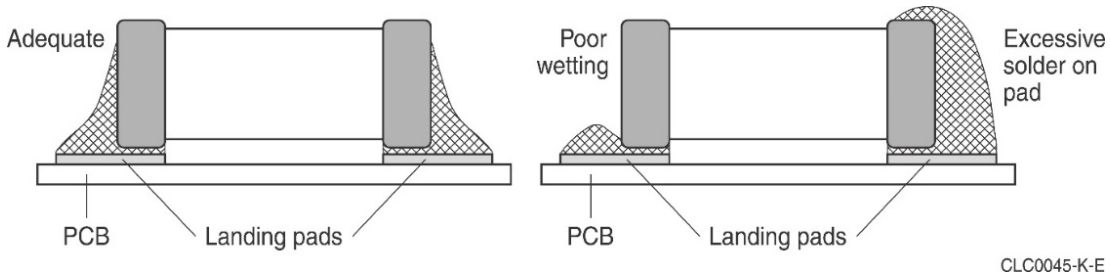
- Please note that the component is designed for reflow soldering. Consult TDK if other soldering processes are considered.
- All temperatures refer to topside of the package, measured on the package body surface.
- Max. number of reflow cycles: 3
- After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.
- The proposed soldering profile is based on IEC 60068-2-58 (respectively JEDEC J-STD-020D) recommendations.

2. Recommended solder

The use of no-clean solder products is recommended. In any case mild, non-activated fluxes should be used. Flux residues after soldering should be minimized.

3. Solder joint profiles

If the meniscus height is too low, that means the solder quantity is too low, the solder joint may break, i.e. the component becomes detached from the joint. This problem is sometimes interpreted as leaching of the external terminations. If the solder meniscus is too high, i.e. the solder quantity is too large, the converse effect may occur. As the solder cools down, the solder contracts in the direction of the component. If there is too much solder on the component, it has no leeway to evade the stress and may break. The figures below show good and poor solder joints for reflow soldering.



4. Notes for proper soldering

4.1. Preheating and cooling

According to IEC 60068-2-58. Please refer to Section Recommended reflow soldering profiles1 of this chapter.

4.2. Repair/ rework

Manual soldering with a soldering iron must be avoided.

4.3. Cleaning

Allow environmentally compatible agents for cleaning only (in case of doubt regarding potential chemical intolerances please contact TDK). Select the appropriate cleaning solution according to the type of flux used. The temperature difference between the components and cleaning liquid must not be greater than 100 °C. Ultrasonic cleaning should be carried out with the utmost caution. Too high ultrasonic power can impair the adhesive strength of the metallized surfaces.

4.4. Solder paste printing

An excessive application of solder paste results in a too high solder fillet, thus making the chip more susceptible to mechanical and thermal stress. Too little solder paste reduces the adhesive strength on the outer electrodes and thus weakens the bonding to the PCB. The solder should be applied smoothly to the end surface.

4.5. Selection of flux

Used flux should have less than or equal to 0.1 wt % of halogenated content, since flux residue after soldering could lead to corrosion of the termination and/or increased leakage current on the surface of the component. Strong acidic flux must not be used. The amount of flux applied should be carefully controlled, since an excess may generate flux gas, which in turn is detrimental to solderability.

4.6. Soldering cautions

CeraLink 2220 components are recommended for reflow soldering. Consult our local representative if other soldering methods are considered.

An excessively long soldering time or high soldering temperature results in leaching of the outer electrodes, causing poor adhesion and a change of electrical properties of the CeraLink due to the loss of contact between electrodes and termination. Keep the recommended down-cooling rate.

Iron soldering must be avoided, hot air methods are recommended for repair purposes.

After the soldering process, the capacitance of CeraLink can be lower. Applying rated voltage V_R to the device will re-establish the capacitance.

5. Solderability tests

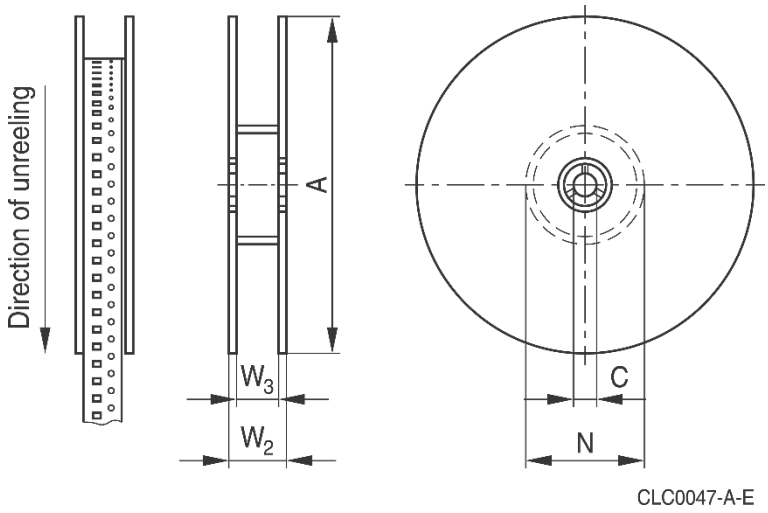
Test	Standard	Test conditions SnPb soldering	Test conditions Pb-free soldering	Criteria
Wettability	IEC 60068-2-58	Immersion in 60/40 SnPb solder using non-activated flux at 215 ±3 °C for 3 ±0.3 s *)	Immersion in SAC solder (Sn96.5Ag3.0Cu0.5 or similar) using non- or low activated flux at 245 ±3 °C for 3 ±0.3 s	Covering of 95% of end termination, checked by visual inspection
Leaching resistance	IEC 60068-2-58	Immersion in 60/40 SnPb solder using mildly activated flux without preheating at 260 ±5 °C for 30 ±1 s *)	Immersion in SAC solder (Sn96.5Ag3.0Cu0.5 or similar) using non- or low activated flux without preheating at 260 ±5 °C for 30 ±1 s	No leaching of contacts
Resistance to soldering heat	MIL-STD-202 Method 210 (Dipping)	Immersion in 60/40 SnPb solder at 260 °C for 10 s. Pre-heating at 150 ºC for 60-120 sec. *)	Immersion in SAC solder (Sn96.5Ag3.0Cu0.5 or similar) at 260 °C for 10 s. Pre-heating at 150 ºC for 60-120 sec. *)	No mechanical damage. $\lvert\Delta C_0/C_0\rvert$, tanδ and R_{ins} within defined limits.
	MIL-STD-202 Method 210 (Reflow)	Three times recommended reflow soldering profile (Pb-free)		No mechanical damage. Proper solder coating of contact areas. $\lvert\Delta C_0/C_0\rvert$, tanδ and R_{ins} within defined limits.

*) These tests can be performed upon customer request

Taping and packing

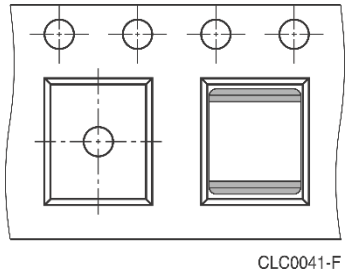
Tape and reel packing in blister according to IEC 60286-3, tape width: 12 ±0.3 mm

Reel packing

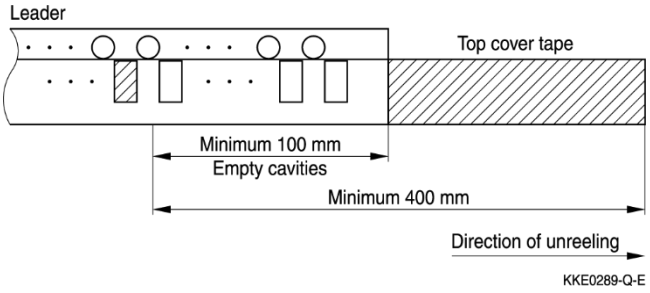


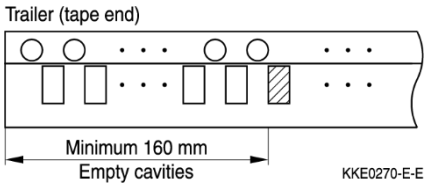
12-mm tape (Dimensions in mm)	
A	180 max.
W_2	18.4 max.
W_3	13.65 ±1.75
C	12.8 min.
N	60 ±1

Part orientation



Leader, trailer





Packing unit

Case size EIA / mm	Packing unit
2220 / 5750	1000 pcs. / reel

General technical information

Storage

- In order to maintain solderability, the components must be stored in a non-corrosive atmosphere. Humidity, temperature, and container materials are critical factors.
- Only store CeraLink capacitors in their original packaging. Do not open the package before storage or prior to processing. Touching the metallization of unsoldered components may change their soldering properties.
- Storage conditions in original packaging: temperature: -25 to +45 °C, relative humidity: ≤ 75% annual average, ≤ 95% on max. 30 days in a year, dew precipitation and wetness are inadmissible.
- Do not store the components where they are exposed to heat or direct sunlight. Otherwise, the packing material may be deformed, or the components may stick together, causing problems during mounting. After opening the factory seals, such as polyvinyl-sealed packages, use the components as soon as possible.
- Avoid contamination of the CeraLink surface during storage, handling, and processing.
- Avoid storing CeraLink devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- The product is recommended to be soldered within 12 months after shipment. Check solderability in case extended shelf life beyond the expiry date is needed.

Handling

- Do not drop CeraLink components or allow them to be chipped.
- Do not touch CeraLink with your bare hands – gloves are recommended.
- Avoid contamination of the CeraLink surface during handling.
- Washing processes to remove e.g. flux are recommended but should be used with caution since they may damage the product due to the possible static or cyclic mechanical loads (e.g. ultrasonic cleaning). Mechanical loads which may cause cracks to develop on the product and its parts must be avoided, since this might lead to reduced reliability or lifetime.

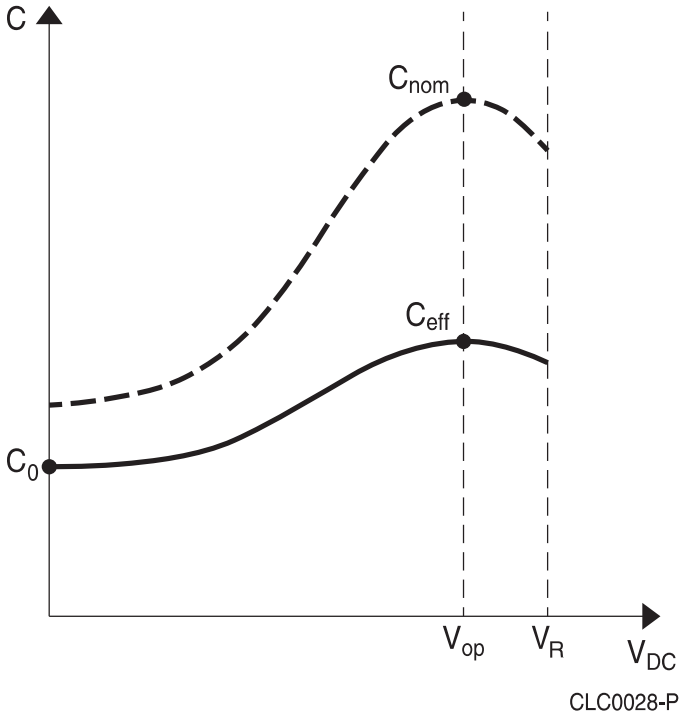
Mounting

- When CeraLink devices are encapsulated with sealing material or overmolded with plastic material, electrical characteristics might be degraded, and the lifetime reduced.
- Board fixation of CeraLink components using SMD adhesives should be avoided. In particular, adhesives with a high Shore hardness and mismatching coefficient of thermal expansion (CTE) might induce cracks in the ceramics. If fixation is not avoidable, adhesives with low Shore hardness and a CTE < 10 ppm/K should be used.
- Make sure the CeraLink component is not damaged before, during or after the mounting process (e.g. during pick and place)
- Avoid high mechanical stress like twisting or bending of the PCB close to the soldered CeraLink.
- Make sure contacts and housings used for assembly with CeraLink components are clean before mounting.
- The surface temperature of an operating CeraLink can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink to allow proper cooling.
- Avoid contamination of the CeraLink surface during processing.

Soldering guidelines

- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.
- If an unfavorable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink may cause damage to the component.
- See chapter *Soldering directions* for further details.

Glossary



Initial capacitance C_0:	Is the value at the origin of the hysteresis without any applied direct voltage.
Effective capacitance C_{eff}:	Occurs at V_{op} and is measured with an applied ripple voltage of 0.5 V AC (RMS) and 1 kHz. The CeraLink is designed to have its highest capacitance value at the operating voltage V_{op}.
Nominal capacitance C_{nom}:	Is the value derived by the tangent of the mean hysteresis (as the derivative of the mean hysteresis is C = dQ/dV).

See our *CeraLink Technical Guide* for further details.

Symbols and terms

AC	Alternating current
C_0	Initial capacitance @ 0 V DC, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{0,\,typ}^{unpoled}$	Initial capacitance C_0 of unpoled component
$C_{eff,\,typ}$	Typical effective capacitance @ V_{op}, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{nom,\,typ}$	Typical nominal capacitance @ V_{op}, quasistatic, +25 °C. See glossary for definition of the nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance @ $V_{pk,max}$, measurement time t = 7 s, +25 °C. For pre- and post-measurements within the scope of the AEC-Q200 reliability tests.
$R_{ins,\,typ}$	Insulation resistance @ V_{op}, measurement time t ≥ 240 s, +25 °C
SAC	Tin silver copper alloy; lead-free solder paste
T_{amb}	Ambient temperature
tanδ	Dissipation factor @ 0 V DC, 0.5 V AC (RMS), 1 kHz, +25°C
T_{device}	Device temperature. $T_{device} = T_{amb} + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
T_{max}	Max. device temperature, T_{max} = +150°C. Reference temperature for reliability tests
V_{op}	Operating voltage at maximum attenuation capability
V_R	Rated voltage. Reference DC voltage for reliability tests.
V AC (RMS)	Root mean square value of sinusoidal AC voltage
$V_{pk,max}$	Maximum peak operating voltage (e.g. voltage overshoots or surge pulses which occur < 5% of total component lifecycle). Not for continuous operation.
ΔT	Increase of temperature during operation

Cautions and warnings

General

- Not for use in resonant circuits, where a voltage of alternating polarity occurs.
- Not for AC applications. Consult our local representative for further details.
- If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.
- Ultimately, it is always the customers' responsibility to check and decide whether this product with the properties described in this data sheet is suitable for use in a specific application in such a way that the risk of a malfunction of the products leading to personal injury or property damage to third parties is excluded.
- Depending on the individual application, CeraLink components are electrically connected to voltages and currents, which are potentially dangerous for life and health of the operator. Installation and operation of CeraLink must be done only by authorized personnel. Ensure proper and safe connections, couplers, and drivers.
- Caution: CeraLink components are highly efficient charge storing devices. Even when disconnected from a supply, the electrical energy content of a loaded component can be high and is held for a long time. Always ensure a complete discharging of the component (e.g. via a 10 kΩ resistor) before handling. Do not discharge by simple short-circuiting, because of the risk of damaging the ceramic.
- Electrical charges can be generated on disconnected components by varying load or temperature. Caution: Discharge a CeraLink before connecting it to a measuring component/electronics, when this component is not sufficiently voltage proved.

  See *Important notes* section for further details.

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the lifetime of CeraLink devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases, the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Operation

- Use CeraLink only within the specified operating temperature range.
- Use CeraLink only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink can produce audible noise due to its piezoelectric characteristic.
- CeraLink components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of the manufacturer.

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The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.tdk-electronics.tdk.com/material). Should you have any more detailed questions, please contact our sales offices.
5. We constantly strive to improve our products. Consequently, **the products described in this publication may change from time to time**. The same is true of the corresponding product specifications. Please check therefore to what extent product descriptions and specifications contained in this publication are still applicable before or when you place an order.

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Important notes

8. The trade names EPCOS, CarXield, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, FilterCap, FormFit, InsuGate, LeaXield, MediPlas, MiniBlue, MiniCell, MKD, MKK, ModCap, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PiezoBrush, PlasmaBrush, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, SurfIND, ThermoFuse, WindCap, XieldCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at www.tdk-electronics.tdk.com/trademarks.

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